ABSTRACT

A processor-memory bus comprises a command portion for transmitting addresses and commands, having a unidirectional input portion for transmitting commands to a central repeater unit, and a unidirectional broadcast portion for broadcasting commands from the repeater. The input portion comprises a plurality of links running from different devices, wherein each link is less than the full width of the broadcast bus portion. A command is transmitted over the input portion in a plurality of bus cycles, and broadcast over the broadcast portion in a single bus cycle. Since multiple input links connect to the central command repeater, it is possible to keep the broadcast bus full notwithstanding the fact that multiple bus cycles are required to transmit an individual command on the input portion. Preferably, the links are arranged hierarchically, from processors to local repeaters, from local repeaters to the central repeater, and back again. Preferably, the central repeater globally arbitrates the bus, and once the bus is granted, the command propagates along each link at pre-defined clock cycles from bus grant. In the preferred embodiment, addresses/commands and data are transmitted on essentially separate paths having different topologies, and at different times, and are arbitrated separately.